



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

Address: COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, Virginia 22313-1450

www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,438	11/12/2003	Torsten Patsch	2003P52601US/1331.102.101	7153
7590 01/16/2009 Dicke, Billig & Czaja, PLLC Fifth Street Towers Suite 2250 100 South Fifth Street Minneapolis, MN 55402				
EXAMINER				
PATEL, KAUSHIKKUMAR M				
ART UNIT		PAPER NUMBER		
2188				
MAIL DATE		DELIVERY MODE		
01/16/2009		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/706,438

Applicant(s)

PARTSCH, TORSTEN

Examiner

Kaushikkumar Patel

Art Unit

2188

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 October 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 and 13-38 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 and 13-38 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-8508)
- Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed October 08, 2008 in response to PTO Office Action mailed July 09, 2008. The applicant's remarks and amendments to the claims and/or specification were considered with the results that follow.
2. In response to last Office Action, claims 1, 31, 34 and 35 have been amended. Claim 12 has been canceled. No claims have been added. As a result, claims 1-11 and 13-28 remain pending in this application.

Response to Arguments

3. Applicant's arguments filed October 08, 2008 have been fully considered but they are not persuasive.

Applicant argues that Watanabe fails to teach or suggest a bypass circuit configured to receive a column address strobe latency select signal (remarks, page 11; paragraph 1). The Examiner respectfully disagrees with the fact. As noted in previous office action (page 3), a combination of control circuit and switch circuit (Watanabe: fig. 4, items 37 and 36) is interpreted as the bypass circuit. The bypass circuit (e.g. combination of switch and control circuit) outputs the data either from the register block (fig. 4, item 35) or bypasses the register block and outputs the data directly from read amplifier (fig. item 34). Here it is noted that the register block is treated as the memory (FIFO) and the data is outputted either from the memory (FIFO) as signal S2 or the

memory is bypassed and data is outputted from sense amplifier (fig. 4, item 34) as signal S1. The bypass circuitry (e.g. control circuit and switch) selects either signal S1 as an output or signal S2 as an output based on column address latency (Watanabe: pars. [0041] – [0044]). The control circuitry generates control signal SC to activate switch based on the CAS latency and therefore it is entirely evident that Watanabe does teach a bypass circuit (e.g. combination of control circuit and switch as shown in fig. 4) and since the control circuit generates control signal SC based on the CAS latency, it must inherently receive signal (e.g. signal based on CAS latency) to determine whether CAS is 1 or higher and therefore it can be inferred that the bypass circuitry receives CAS latency select signal.

The Applicant further argues that tri-state buffer and memory using FIFO are not capable of instant and unquestionable demonstration as being well known and therefore according to MPEP § 2144.03 (A), the Examiner's official notice is improper. The Examiner respectfully disagrees with the fact, because a simple search using term "FIFO buffer" in EAST database produced nearly 14,000 hits and term "tri-state buffer" produced nearly 1500 hits. It is further noted that, the Office action mailed on December 12, 2007 cited some references as evidentiary support for use of FIFO buffer and tri-state output buffer (page 11, item 23). The Examiner is also providing some additional references to support the Examiner's assertion of Official Notice in prior office action. Saeki et al. (A 2.5-ns Clock Access, 250-MHz, 256-Mb SDRAM with Synchronous Mirror Delay, published by IEEE journal of solid state circuits, vol. 31, November 1996) teaches (figs. 5 and 6, page 1659) SDRAM with register block arranged into FIFO

configuration (e.g. similar to Watanabe). Saeki also teaches that the FIFO consists of five registers for CAS latency (CTL) = 5 (page 1660, sect. B. "Simple Controlling of FIFO with parallel serial converter"). Sredanovic (US 5,959,899) teaches DRAMs and SRAMs with FIFO buffer (col. 1, lines 11-29) and tri-state output buffer (col. 2, lines 57-67) are well known in the art. Similarly, Emberling (US 7,184,508) and Au (US 7,330,991) teaches DDR SDRAM with output including FIFO buffer (col. 1, lines 15-38). Chang et al. (US 5,500,818) teaches memory with tri-state buffer as output (fig. 2a, col. 5, lines 17-34).

Applicant further argues that Watanabe discloses signal S1 and S2 and they are data signals, but they do not latch data according to claim 17 (remarks, page 12). Here it is noted that the interpretation is consistent with the Applicant's disclosure. As per Applicant's disclosure (abstract, lines 4-7): "a circuit is configured to select between receiving data from the memory to provide first output signals and receiving data from the bypass circuit to provide second output signals based on the column address strobe latency signal". Applicant's disclosure further disclose (page 9, lines 25-27): "The bREADY pulse at 204 latches the data at 206 into a latch, indicated at 252, which is the FIFO memory block 104 input." The Examiner is not able to find any further reference to the first and second signals in the disclosure, therefore the data signals S1 and S2 are consistent with the Applicant's disclosure and latching data from FIFO to the output pad is considered as latching first signals or second signals as output based on the CAS latency.

Applicant further argues that DDR-I SDRAM, DDR-II SDRAM and low power SDRAM are not well known in the art (remarks, page 13). The Examiner respectfully disagrees with the fact because as per Applicant's own disclosure, above mentioned memories are well known in the art (page 1, background of the invention section, lines 7-9 and lines 27-28), "one type of memory known in the art is double data rate synchronous dynamic random access memory (DDR SDRAM)"; "One type of DDR SDRAM is Mobile DDR SDRAM. Mobile DDR SDRAM is a new generation of low power SDRAM designed especially for mobile applications". It is also noted that the final office action mailed on December 12, 2007 (page 12) cited various references teaching kinds of memory structures claimed by the Applicant.

Applicant further argues that Edo, Hamamoto and Matsudera do not teach rise and fall circuitry that controls the timing of rise and fall control signals (remarks, page 14). Here it is noted that rise and fall circuits are utilized to serialize the data access which is entirely evident from the Applicant's disclosure and the claim language (e.g. claims 6 and 9). As noted in previous office action, page 8, Edo, Hamamoto and Matsudera teach serializing data according to rise and fall edges of the clock, where it is readily apparent that it requires a circuit to control the signals. It is further noted that according to MPEP § 2106: "USPTO personnel must always remember to use the perspective of one of ordinary skill in the art. Claims and disclosures are not be evaluated in a vacuum. If elements of an invention are well known in the art, the applicant does not have to provide a disclosure that describes those elements". Based on above, the Examiner believes that the well known elements (e.g. rise/fall circuits) are

not fully disclosed in above cited references, however they serializes the data access based on the rising and falling edges of the clock signals, which is what the Applicant is trying to achieve. Akioka et al. (A 6-ns 256-kb BiCMOS TTL SRAM, published by IEEE Journal of solid-state circuits, vol. 26, March 1991) teaches the SRAM memory with output circuit including a circuit to control rise/fall times of the output (page 441, fig. 6, sec. C. "Two-level-presetting TTL Output Buffer").

Applicant further argues that Watanabe teaches a single memory cell storing a single data bit and therefore there is rising and falling edge data bits to strobe out and thus one having ordinary skill in the art would not add rise/fall circuit (remarks, pages 14, 15). The Examiner respectfully disagrees with the fact. As noted in previous office action (page 3), claim 1 of the Watanabe is cited, which claims "memory cells for storing data". Here it is noted that all the cells in the memory array works similar to single cell and therefore Watanabe describes one cell for the illustration purpose, however the actual invention is claimed in the claims and the claims recite memory having multiple cells. This is also evident from fig. 2 of the applicant, which clearly shows a single cell, therefore it can be inferred that the applicant is also using single cell. It is also noted that the data is read from the memory by one cell at a time, e.g. each bit is read by combination of row address and the column address and single bit is outputted from single cell and then all the bits are combined at the output. It is further noted that the data output is synchronized with the system clock and the system clocks rises and falls and the output of data bits must be matched with the rising and falling edge of the clock and thus the output of bits does not have to have rising and falling edges but instead it

is associated with the clock and which rises and falls and the output must be synchronized/serialized with the clock. Thus, Applicant's arguments are not persuasive and the rejection of the claims are maintained and reiterated below for the Applicant's convenience.

Admitted Prior Art

4. As shown above, the noticed facts (well known in the art) are capable of instant and unquestionable demonstration as being well-known and the Applicant has failed to adequately traverse the Examiner's assertion of the Official Notice the facts are considered as admitted prior art. According to MPEP 2144.03 (C):

"To adequately traverse such a finding, an applicant must specifically point out the supposed errors in the examiner's action, which would include stating why the noticed fact is not considered to be common knowledge or well-known in the art. See 37 CFR 1.111(b). See also Chevenard, 139 F.2d at 713, 60 USPQ at 241 ("[I]n the absence of any demand by appellant for the examiner to produce authority for his statement, we will not consider this contention."). A general allegation that the claims define a patentable invention without any reference to the examiner's assertion of official notice would be inadequate. If applicant adequately traverses the examiner's assertion of official notice, the examiner must provide documentary evidence in the next Office action if the rejection is to be maintained. See 37 CFR 1.104(c) (2). See also Zurko, 258 F.3d at 1386, 59 USPQ2d at 1697 ("[T]he Board [or examiner] must point to some concrete evidence in the record in support of these findings" to satisfy the

substantial evidence test). If the examiner is relying on personal knowledge to support the finding of what is known in the art, the examiner must provide an affidavit or declaration setting forth specific factual statements and explanation to support the finding. See 37 CFR 1.104(d) (2). If applicant does not traverse the examiner's assertion of official notice or applicant's traverse is not adequate, the examiner should clearly indicate in the next Office action that the common knowledge or well-known in the art statement is taken to be admitted prior art because applicant either failed to traverse the examiner's assertion of official notice or that the traverse was inadequate. If the traverse was inadequate, the examiner should include an explanation as to why it was inadequate.

Since the Applicant asking for the reference and not providing any reasoning and/or errors that why noticed facts can not be combined or used with Watanabe, the noticed facts is treated as admitted prior art, the facts are the outputs of memory as first-in first-out buffers and FIFO memories are well known in the art.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-3, 13-18, 24, 31, 32, 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (US 2001/0017790).

As per claim 1, Watanabe teaches a random access memory (par. [0002]), comprising:

an array of memory cells (par. [0003], see claim 1);

a memory configured to receive data from the array of memory cells (fig. 4, item 35);

a bypass circuit (fig. 4, items 36, 37) configured to receive a column address strobe latency select signal (Watanabe expressly fail to teach this limitation, however it is noted that the control circuit selects output from the register block or bypasses the register block and selects output from read amplifier 34 based on the CAS latency (pars. [0041] - [0044]), where it is readily apparent that an indication (e.g. CAS latency select signal) must be provided to the circuit based on which the circuits outputs the data) the data from the array of memory cells and to bypass the memory (fig. 4, item P1; par. [0038]); and

a circuit (fig. 4, items 36, 37) configured to select between receiving the data from the memory to provide first output signals (fig. 4, S2) and receiving the data from the bypass circuit to provide second output signals (fig. 4, S1) based on a column address strobe latency select signal (pars. [0017], [0041]).

Watanabe teaches bypass circuit with output (fig. 4, S1) with two states (e.g. 0 and 1), but fails to teach tri-state output as required by the claim. However, the use of tri-state output is well known in the art and the examiner takes official notice of the fact. Thus, it would have been obvious to one having ordinary skill in the art at the time of the invention to use tri-state output, because tri-state output provides three states (e.g. low

(0), high (1) and Hi-Z (or off)), wherein the third state (Hi-Z) isolates (turns off) the floating output from the circuit, which allows multiple circuits to use same output (e.g. when CAS latency is greater than one, the Hi-Z state isolates the output from bypass circuit, allowing output from FIFO circuit to pass data). (It is noted here that various references are cited above in response to argument section using tri-state buffer as an output).

As per claim 2, Watanabe teaches, wherein the circuit is configured to receive the data from the bypass circuit and provide the second output signals if the column address strobe latency select signal indicates a column address strobe latency value of one (par. [0044]).

As per claim 3, Watanabe teaches, wherein the circuit is configured to receive the data from the memory and provide the first output signals if the column address strobe latency select signal indicates column address strobe latency value of greater than one (par. [0044]).

As per claim 13, Watanabe teaches a memory (e.g. register block) for storing data received from an array of memory cells (see claim 1 above). Watanabe fails to teach memory is a first in first out memory (FIFO), however the use of FIFO for storing data is well known in the art and the examiner takes official notice of the fact. Thus, it would have been obvious to one having ordinary skill in the art at the time of the

invention to utilize FIFO memory instead of register blocks in the system of Watanabe because FIFO storage allows easier flow control and maintains the program order to avoid any false data access.

As to claims 14, 15 and 16, Watanabe teaches synchronous random access memory (SDRAM) (par. [0002]), but fails to teach low power SDRAM, a double data rate-I (DDR) SDRAM and DDR-II SDRAM. However, the technology of a low power SDRAM as well as DDR-I and DDR-II SDRAM is well known in the art (see applicant's disclosure, page 1, lines 7-29) and the examiner takes official notice of the fact. Thus, it would have been obvious to use a low power SDRAM, DDR-I SDRAM and DDR-II SDRAM in the system of Watanabe to reduce the power consumption and/or increase the data retrieval speed.

As per claim 17, Watanabe teaches a random access memory (par. [0002], comprising:

- a memory (fig. 4, item 35);
- a bypass circuit that bypasses the memory (fig. 4, item P1, par. [0038]); and
- a control circuit (fig. 4, item 37) configured to provide first signals (fig. 4, item S2) and second signals (fig. 4, item S1), wherein the first signals latch data from the memory to provide a column address strobe latency of greater than one and the second signals latch data from the bypass circuit to provide a column address strobe latency of one (pars. [0017], [0044]).

Watanabe teaches the memory is a register block (fig. 4, item 35), but fails to teach first in first out memory (FIFO). The use of FIFO for storing data is well known in the art and the examiner takes official notice of the fact. Thus, it would have been obvious to one having ordinary skill in the art at the time of the invention to utilize FIFO memory instead of register blocks in the system of Watanabe because FIFO storage allows easier flow control and maintains the program order to avoid any false data access.

As per claim 18, Watanabe teaches, wherein the control circuit comprises a clock signal multiplexer configured to select between providing the first signals and the second signals based on a column address strobe latency select signal (fig. 4, items 36 and 37, pars. [0038], [0041], [0044], the control circuit and switching circuit selects between S1 and S2 based on CAS latency value, which means control and switching circuits can be considered as clock signal multiplexer).

Claim 24 is rejected under same rationales as applied to claim 12 above.

As per claim 31, Watanabe teaches a random access memory (par. [0002], claim 1) comprising:

means for storing data read from an array of memory cells (fig. 4, item 35);

means for receiving the data read from the array of memory cells to bypass the

means for storing data (fig. 4, item P1, par. [0038];

means for retrieving the data from the means for storing the data if column address strobe latency is greater than one (par. [0044]);

means for retrieving the data from the means for receiving the data if the column address strobe latency is one (par. [0044]).

Watanabe teaches bypass circuit with output (fig. 4, S1) with two states (e.g. 0 and 1), but fails to teach tri-state output as required by the claim. However, the use of tri-state output is well known in the art and the examiner takes official notice of the fact. Thus, it would have been obvious to one having ordinary skill in the art at the time of the invention to use tri-state output, because tri-state output provides three states (e.g. low (0), high (1) and Hi-Z (or off)), wherein the third state (Hi-Z) isolates (turns off) the floating output from the circuit, which allows multiple circuits to use same output (e.g. when CAS latency is greater than one, the Hi-Z state isolates the output from bypass circuit, allowing output from FIFO circuit to pass data). (It is noted here that various references are cited above in response to argument section using tri-state buffer as an output).

Claim 32 is rejected under same rationales as applied to claim 13 above.

As per claim 34, Watanabe teaches a method for reading data from a random access memory in a column address strobe latency of one (par. [0011], comprising: initiating a read command on a first edge of a clock cycle (pars. [0011], [0064]);

receiving data read from the array of memory cells in a bypass circuit during the clock cycle (pars. [0011], [0064]); and

retrieving the data from the bypass circuit during the clock cycle (pars. [0011], [0064]).

Watanabe teaches the memory is a register block (fig. 4, item 35), but fails to teach first in first out memory (FIFO). The use of FIFO for storing data is well known in the art and the examiner takes official notice of the fact. Thus, it would have been obvious to one having ordinary skill in the art at the time of the invention to utilize FIFO memory instead of register blocks in the system of Watanabe because FIFO storage allows easier flow control and maintains the program order to avoid any false data access.

Watanabe teaches bypass circuit with output (fig. 4, S1) with two states (e.g. 0 and 1), but fails to teach tri-state output as required by the claim. However, the use of tri-state output is well known in the art and the examiner takes official notice of the fact. Thus, it would have been obvious to one having ordinary skill in the art at the time of the invention to use tri-state output, because tri-state output provides three states (e.g. low (0), high (1) and Hi-Z (or off)), wherein the third state (Hi-Z) isolates (turns off) the floating output from the circuit, which allows multiple circuits to use same output (e.g. when CAS latency is greater than one, the Hi-Z state isolates the output from bypass circuit, allowing output from FIFO circuit to pass data). (It is noted here that various references are cited above in response to argument section using tri-state buffer as an

Art Unit: 2188

output).

As per claim 35, Watanabe teaches the method of claim 34, comprising bypassing first in/first out memory cells used to provide data if the column address strobe latency is one (par. [0044]).

7. Claims 4-11, 19-23, 33 and 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (US 2001/0017790) as applied to claims 1, 17, 31 and 34 above, and further in view of Edo (US 6,282,150) and/or Hamamoto et al. (US 6,417,715) and/or Matsudera et al. (US 6,801,144).

As per claims 4 and 6, Watanabe teaches all the limitations of claim 1, but fails to teach first and second rise and fall circuits respectively for the memory and bypass circuits. Edo teaches a semiconductor memory outputting data synchronously with the rise and fall phases of the reference clock one bit at a time (Edo, abstract, col. 1, lines 6-32). Hamamoto teaches semiconductor memory device using clock generation circuit that generates internal clocks based on external reference clocks to serialize data output with rising and falling edges of the clock (Hamamoto, abstract, col. 1, lines 10-32; col. 2, lines 9-25). Matsudera teaches rise and fall circuits for serializing input/output bits to/from memory cells (Matsudera, abstract, col. 7, lines 36-61). It would have been obvious to one having ordinary skill in the art at the time of the invention to use rise and fall circuits (first and second, each for FIFO memory and bypass circuit) as taught by

Art Unit: 2188

Edo, Hamamoto and Matsudera in the system of Watanabe to serialize and/or synchronize data access to improve the performance of the memory.

As per claims 5 and 7, Watanabe, Edo, Hamamoto and Matsudera teach wherein the circuit is configured to provide the first rise and fall signals after a first clock cycle is completed following a read command that is initiated by a first edge of the first clock cycle (Watanabe teaches providing signal after the read command is issued, pars. [0011], [0064]. As explained above (claims 4 and 6), the rise and fall signals are also applied to serialize and/or synchronize data access one bit at a time).

As per claim 8, Watanabe teaches wherein the circuit comprises a multiplexer configured to select between serialized data from the first circuit and serialized data from the second circuit based on the column address strobe latency select signal (fig. 4, items 36 and 37, pars. [0038], [0041], [0044], the control circuit and switching circuit selects between S1 and S2 based on CAS latency value, which means control and switching circuits can be considered as clock signal multiplexer).

Claims 9 and 10 rejected under same rationales as applied to claims 4-7 above.

As per claim 11, the sequence of applying various signals is inherent in the combined system of Watanabe, Edo, Hamamoto and Matsudera, otherwise the system

will provide wrong data and it will fail because without proper synchronization of all the signals the data output will be erroneous.

Claim 19 is rejected under same rationales as applied to claims 4 and 6 above.

As per claim 20, Hamamoto and Edo teach wherein the control circuit is configured to provide the first signals comprising a first rise signal and a first fall signal that is the inverse of the first rise signal and the second signals comprising a second rise signal and a second fall signal that is the inverse of the second rise signal (Hamamoto, col. 4, lines 15-18; Edo, col. 17, lines 18-45).

As per claim 21, Edo teaches wherein the rise/fall circuit is configured to provide a first data bit as output on a rising edge of the first rise signal and a second data bit as output on arising edge of the first fall signal (Edo, col. 18, lines 15-18).

As per claim 22, Hamamoto teaches comprising a data delay circuit electrically coupled to the rise/fall .circuit and configured to adjust output timing of the data (Hamamoto, fig. 2, items 130 and 150).

As per claim 23, Watanabe, Edo, Hamamoto and Matsudera explicitly fail to teach driver to pass data from the delay circuit to a data pad, however the driver is inherent in the system to provide data at output data pad.

Claim 33 is rejected under same rationales as applied to claims 4 and 6.

Claims 36-38 are rejected under the same rationales as applied to claims 20-23.

8. Claims 25-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (US 2001/0017790) and further in view of Edo (US 6,282,150) and/or Hamamoto et al. (US 6,417,715) and/or Matsudera et al. (US 6,801,144).

As per claim 25, Watanabe teaches a random access memory, comprising:

a memory circuit (fig. 4, item 35);

a bypass circuit configured to bypass the memory circuit (fig. 4, item P1, par. [0038]).

Watanabe further teaches a first output signal (fig. 4, item S2) and a second output signal (fig. 4, item S1) and a multiplexer configured to select between the first output signal and the second output signal based on a column address strobe latency select signal (fig. 4, items 36 and 37, pars. [0017], [0038], [0044]).

Watanabe fails to teach a first rise/fall circuit configured to receive data from the memory circuit and a second rise/fall circuit configured to receive data from the bypass circuit. Edo teaches a semiconductor memory outputting data synchronously with the rise and fall phases of the reference clock one bit at a time (Edo, abstract, col. 1, lines 6-32). Hamamoto teaches semiconductor memory device using clock generation circuit that generates internal clocks based on external reference clocks to serialize data output with rising and falling edges of the clock (Hamamoto, abstract, col. 1, lines 10-32;

Art Unit: 2188

col. 2, lines 9-25). Matsudera teaches rise and fall circuits for serializing input/output bits to/from memory cells (Matsudera, abstract, col. 7, lines 36-61). It would have been obvious to one having ordinary skill in the art at the time of the invention to use rise and fall circuits (first and second, each for FIFO memory and bypass circuit) as taught by Edo, Hamamoto and Matsudera in the system of Watanabe to serialize and/or synchronize data access to improve the performance of the memory.

Claims 26-30 are also rejected under same rationales as applied to claims 4-8 and 19-23 above.

Conclusion

9. The examiner also requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line no(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

10. When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The references are cited to show the well known facts relied upon by the Examiner in previous office action (see response to argument section above).

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaushikkumar Patel whose telephone number is (571)272-5536. The examiner can normally be reached on 7.30 am - 4.00 pm.

Art Unit: 2188

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hyung S. Sough/
Supervisory Patent Examiner, Art Unit 2188
01/15/09

Kaushikkumar Patel
Examiner
Art Unit 2188

/kmp/